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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/427,114
Filing Date: October 26, 1999
Appellant(s): OBARA ET AL.

Ellen Marcie Emas, Reg No. 32131
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed August 10, 2006 appealing from the Office action mailed January 10, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1-9, 11-19 and 21-26.

Claims 10 and 20 been canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,630,135	Orimo et al.	5-1997
5,790,842	Charles et al.	8-1998

FOLDOC, http://foldoc.doc.ic.ac.uk/foldoc/foldoc.cgi?query=image, October 21, 1994.

Merriam-Webster's Collegiate Dictionary, Tenth Edition, 2001, pages 72 and 1192.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orimo et al., U.S. Patent Number 5,630,135 (herein referred to as Orimo) in view of Charles et al., US Patent 5,790,842 (herein referred to as Charles).

3. Referring to claim 26, Orimo has taught an image processing device comprising:

a. a first image processor for executing first image processing in image data (Orimo, figure 1, column 2, lines 1-25, one of the first processors, column 11, lines 18-21);

b. a second image processor for executing second image processing on said image data that was subjected to the first image processing (Orimo, figure 1, column 2, lines 1-25, second processor, column 11, lines 18-21); and

c. a memory for storing said image data in association with state information to represent the processing state of said image data (Orimo, figure 5, element 306, column 5, lines 1-12), wherein

d. said first and second image processings are asynchronously executed on said image data by said first and second image processors (Orimo, column 2, lines 9-16, column 11, lines 2-20, Asychronous is defined by Merriam-Webster as "not synchronous". Synchronous is defined as "happening, existing, or arising at precisely the same time". So asynchronous is interpreted as not happening at the same time. In Orimo a first processing is executed in a first processor and the data results are sent to the second processor via a message. The second processor selects a message and executes a second processing using the selected message. A first processing is executed and then a second processing is executed. The second processing is executed after the first processing. The first and second processings do not happen, or execute, at the same time. Therefore the first and second processings of Orimo are asynchronous executed.)

4. Orimo has not specifically taught said first and second image processors share said memory. However, Charles has taught image data processors sharing a common memory. Charles has further taught that having a shared memory eliminates the need for separate memory devices in multiple processing systems and thus permits a more efficient and cost effective processing system implementation (Charles, Column 27, lines 53-63). Therefore it would have been obvious to one of ordinary skill in the art at

the time the invention was made to have the first and second image processors of Orimo share a memory, as taught by Charles, for the desirable purpose of eliminating the need for separate memory devices for each processor and thus permit a more efficient and cost effective processing system implementation (Charles, Column 27, lines 53-63).

5. Claim 25 does not recite limitations above the claimed invention set forth in claim 26 and is therefore rejected for the same reasons set forth in the rejection of claim 26 above.

6. Claims 1-9, 11-19 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orimo et al., U.S. Patent Number 5,630,135 (herein referred to as Orimo) in view of http://foldoc.doc.ic.ac.uk/foldoc/foldoc.cgi?query=image (herein referred to as FOLDOC), and Charles et al., US Patent 5,790,842 (herein referred to as Charles).

7. Referring to claim 1, Orimo has taught a data processing system comprising:

a. a plurality of processors for executing a series of different types of processing functions on data to be processed (Orimo, figure 1, column 2, lines 1-25, a first processor and a second processor, column 11, lines 2-21) in a prescribed order (Orimo, column 2, lines 1-25, A first processing executes a first type of processing. The second processor processes a second type of processing on the data after the first processing.) each processor executing a processing function different from one another (see column 11, lines 5, 6 and 17-20 which explains that the first processor executes one of the multi-version programs and

the second processor executes a program other than one of the multiple-version programs.) and said data to be processed being image data that consists of a plurality of pixel data (abstract, column 10, lines 31-36, column 12, lines 60-65, Orimo has taught an image in a computer, or a digital image. Orimo has not specifically stated that the digital image consists of a plurality of pixel data. However, FOLDOC supports that a digital image is composed of a plurality of pixels.) ; and

b. a memory for storing said data to be processed in association with state information to represent the processing to be performed next for each pixel data of said data to be processed (Orimo, figure 5, element 306, column 5, lines 1-12), wherein

c. said processing functions are asynchronously executed on said data to be processed by said plurality of processors (Orimo, column 2, lines 9- 16, column 11, lines 2-20, Asychronous is defined by Merriam-Webster as "not synchronous". Synchronous is defined as "happening, existing, or arising at precisely the same time". So asynchronous is interpreted as not happening at the same time. In Orimo, a first processing is executed in a first processor and the data results are sent to the second processor via a message. The second processor selects a message and executes a second processing using the selected message. A first processing is executed and then a second processing is executed. The second processing is executed after the first processing. The first and second processings do not happen, or execute, at the same time.

Therefore the first and second processings of Orimo are asynchronous executed.) one processing is executed on each pixel data by one of the processors at a time (column 2, lines 1-49, pixel data is executed in the first and second processors, column 11, lines 2-20).

8. Orimo et al. have not specifically taught that said plurality of processors share said memory. However, Charles has taught image data processors sharing a common memory. Charles has further taught that having a shared memory eliminates the need for separate memory devices in multiple processing systems and thus a more efficient and cost effective processing system implementation (Charles, Column 27, lines 53-63). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the processors of Orimo share a memory, as taught by Charles, for the desirable purpose of eliminating the need for separate memory devices for each processor and thus permit a more efficient and cost effective processing system implementation (Charles, Column 27, lines 53-63).

9. Referring to claim 2, Orimo has taught the data processing system according to claim 1, wherein the plurality of processors each determine if said data to be processed can be processed based on said state information (Orimo, column 4, lines 4-9, column 5, lines 27-39).

10. Referring to claim 3, Orimo has taught the data processing system according to claim 2, wherein the plurality of processors each execute a processing on said data to be processed, and then rewrite said state information corresponding to the processed data (Orimo, column 7, lines 54-56).

11. Referring to claim 4, Orimo has taught the data processing system according to claim 1, further comprising a first controller for controlling said plurality of processors to execute said series of processing functions based on said state information (Orimo, figure 1, element 100, column 4, lines 4-9, column 5, lines 27-39, Each processor controls itself to execute the processings based on state information and each individual control cooperates with the control of the other processors to provide control for the entire system.).

12. Referring to claim 5, Orimo has taught the data processing system according to claim 4, wherein said first controller rewrites said state information corresponding to processed data in response to the completion of each processing by said plurality of processors (Orimo, figure 1, element 100, column 7, lines 54-56, Each processor controls itself to rewrite state information upon completion of each processing and each individual control cooperates with the control of the other processors to provide control for the entire system.).

13. Referring to claims 6 and 7, Orimo has taught the data processing system according to claim 1, further comprising a second controller for determining an attribute of said data to be processed (Orimo, column 5, lines 39-49), wherein said second controller rewrites said state information corresponding to said data to be processed in order to change the order of executing said series of processings if it is determined that said data to be processed has a prescribed attribute (Orimo, column 8, lines 46-66).

14. Referring to claim 8, Orimo has taught the data processing system wherein said memory has one region to store said state information corresponding to a single region where data to be processed is stored (Orimo, figure 2, elements 201 and 205).

15. Referring to claim 9, Orimo has taught the data processing system wherein said memory has one region to store said state information corresponding to a plurality of regions where data to be processed is stored (Orimo figure 5, elements 3060 and 3063).

16. Claims 11- 16, and 18-19 do not recite limitations above the claimed invention set forth in claims 1-6 and 8-9 and are therefore rejected for the same reasons set forth in the rejections of claims 1-6 and 8-9 above.

17. Referring to claim 17, Orimo has taught the data processing system according to claim 16, wherein said second control means rewrites said state information corresponding to said data to be Processed in order to remove a part of said series of processing functions, if it is determined that said data to be processed has a prescribed attribute (Orimo, column 6, lines 16-43, The process must be removed from the series of processings in order to execute.).

18. Referring to claim 21, Orimo in Combination with Charles and FOLDOC have taught the data processing system of claim 1, as described above, and wherein a given data item is stored at the same location in said memory after each of said plurality of processing functions is performed on said given data item (Charles, Column 27, lines 53-63).

19. Referring to claim 22, Orimo in Combination with Charles and FOLDOC have taught the data processing system of claim 21, as described above, and wherein the state information for said given data item is stored at the same location in said memory after each of said plurality of processing functions is performed on said given data item (Charles, Column 27, lines 53-63).

20. Claims 23 and 24 do not recite limitations above the claimed invention set forth in claims 21 and 22 and are therefore rejected for the same reasons set forth in the rejections of claims 21 and 22 above.

(10) Response to Argument

1) On page 9, 2nd and 3rd paragraphs of the Appeal Brief, Appellant argues in essence:

> *"Orimo et al. is directed to a multiple-execution method of multiple-version programs (i.e. a plurality of programs for performing the same function but having different program structures). Figures 8 and 9 of Orimo show processors 12 and 13 perform the same simulation using different versions while Figure 10 shows processors 11-13 perform the same function using different versions (col. 1, lines 18-20, col. 7, lines 59-67, col. 9 lines 6-19, 55-67). Since processors 12-13 in Figures 8 and 9 and processors 11-13 in Figure 10 performs the same function, nothing in Orimo et al. shows, teaches or suggests each processor executes a processing function different from one another as claimed in claims 1 and 11. Rather, Orimo teaches away from the claimed invention since processors 12-13 in Figures 8 and 9 and processors 11-13 in Figure 10 perform the same type of processing functions. Additionally, since Orimo discloses that processors 12-13 in Figures 8-9 and processors 11-13 in Figure 10 perform the same function, nothing in Orimo et al. shows, teaches or suggests that each processor executes a processing function different from one another as claimed in claims 1 and 11. Rather, Orimo et al. teaches away from the claimed invention since the processors perform the same function but have different program structures."*
>
> Orimo has in fact taught that *each processor executes a processing function different from one another as claimed in claims 1 and 11*. As an initial matter, Examiner notes that the cited sections of Orimo in the argument above (*Figures*

8, 9 and 10, processors 11-13, col. 1, lines 18-20, col. 7, lines 59-67, col. 9 lines 6-19, 55-67) have **not** been cited and relied upon in the rejection for claims 1 or claim 11. Appellant has not directly responded to the rejection of the claims on appeal. Furthermore, column 11, lines 2-20 of Orimo makes it clear that each processor, i.e. the claimed first and second processors, executes a processing function different from one another as claimed. Specifically see column 11, lines 5, 6 and 17-20 which explains that the first processor executes one of the multi-version programs and the second processor executes a program other than one of the multiple-version programs. Thus each processor executes a processing function different from one another, one processor executes one of the multiple-version programs and the other processor executes some other program. Also see the Final rejection, page 3, line 8-page 4, line 8. Therefore this argument is moot.

2) On the last paragraph of page 9, Appellant argues in essence:

"Also, Orimo discloses in Figure 9 and column 9, lines 6-19, that both processors 14 and 15 receive messages from the processors 12 and 13. Thus nothing in Orimo et al. shows, teaches or suggests one processing is executed on each pixel data by one of the processors at a time as claimed in claims 1 and 11. Rather, Orimo et al. teaches away from the claimed invention since both processors 14 and 15 in Figure 9 process the data messages 520a, 520b from processors 12 and 13."

However, examiner notes that the cited sections of Orimo in the argument above *(Figure 9, column 9, lines 6-19, processors 12, 13, 14 and 15, data messages 520a, 520b)* are **not** relied upon anywhere in the rejection for the claims on appeal. Appellant has not directly responded to the rejection of the claims on

appeal. Furthermore, Orimo has taught one processing is executed on each pixel data by one of the processors at a time, as claimed in claims 1 and 11. With this limitation, Appellant has merely claimed that for each pixel data there is some point in time where the pixel data is executed by at least one of the processing means. i.e. each pixel data gets executed. Appellant appears to be reading limitations into the claims that are not present. Appellant has not claimed "**only** one processing is executed ... at a time." Since Orimo has taught executing each claimed pixel data (column 2, lines 1-25, column 11, lines 2-20, The pixel data executed in the first processor and the second processor.), then Orimo has in fact taught that one processing is executed on each pixel data by one of the processors at a time as claimed in claims 1 and 11. Therefore this argument is moot.

3) On page 10, lines 3-7 and page 11, lines 14-17 of the Appeal Brief, Appellant argues in essence:

> *"Finally, Orimo et al. merely discloses that processors 11-13 process data in parallel (col. 8, lines 34-37, col. 10 lines 11-13 and 50-54). Nothing in Orimo et al. shows, teaches or suggests processing functions are asynchronously executed as claimed in claims 1 and 11. Rather, Orimo et al. merely discloses processing data in parallel.*
>
> ...
>
> *Furthermore, Orimo et al. merely discloses processors are executed in parallel. Nothing in Orimo et al. shows, teaches or suggests first and second processing are asynchronously executed as claimed in claims 25 and 26. Rather, Orimo et al. only discloses that the processors are executed in parallel."*

However, examiner notes that the cited sections of Orimo in the argument above *(col. 8, lines 34-37, col. 10 lines 11-13 and 50-54)* are **not** relied upon anywhere in the rejection of the claims on appeal. Appellant has not directly responded to

the rejection for the claims on appeal. Furthermore, Appellant has not provided any special meaning of asynchronous anywhere in the claims or in the specification. Since asynchronous has not been given a special meaning, then the term may be given its broadest reasonable interpretation consistent with the specification, see MPEP 724(2)(ii), 904.01. Asychronous is defined by Merriam-Webster as "not synchronous". Synchronous is defined as "happening, existing, or arising at precisely the same time". So asynchronous is interpreted as not happening at the same time. In Orimo (column 11, lines 2-20), a first processing is executed in a first processor and the data results are sent to the second processor via a message. The second processor selects a message and executes a second processing using the selected message. A first processing is executed and then a second processing is executed. The second processing is executed after the first processing. The first and second processings do not happen, or execute, at the same time. Therefore the first and second processings of Orimo are asynchronous executed as claimed in claim 25 and 26. Therefore this argument is moot.

4) On page 10, lines 8-15 of the Appeal Brief, Appellant argues in essence:

"FOLDOC merely discloses a digital image is composed of pixels arranged in a rectangular array with a certain height and width. Nothing in FOLDOC shows, teaches or suggests a) each processor executes a processing function different from one another, b) a plurality of processors executing a series of different types of processing functions, c) one processing is executed at a time on each pixel by one of the processors or d) processing functions are asynchronously executed as claimed in claims 1 and 11. Rather, FOLDOC merely discloses a digital image is composed of pixels arranged in a rectangular array."

However FOLDOC was not relied upon for having taught the argued limitations above in claims 1 and 11. FOLDOC was **not** cited for teaching *a) each processor executes a processing function different from one another, b) a plurality of processors executing a series of different types of processing functions, c) one processing is executed at a time on each pixel by one of the processors or d) processing functions are asynchronously executed as claimed in claims 1 and 11.* FOLDOC was merely cited for teaching that digital images are pixel data. Therefore this argument is moot.

5) On page 10, lines 16-22 and page 11, lines 18-21 of the Appeal Brief, Appellant argues in essence:

> *"Charles et al. is directed to a memory arbitration technique which allows multiple processes to share a common memory device. Nothing in Charles et al. shows, teaches or suggests a) each processor executing a processing function different from one another, b) a plurality of processors executing a series of different types of processing functions, c) one processing is executed at a time on each pixel by one of the processors or d) processing functions are asynchronously executed as claimed in claims 1 and 11.*
>
> ...
>
> *As discussed above, Charles et al. merely discloses a shared memory device. Nothing in Charles et al. shows, teaches or suggests a) second processing on data to be processed that was subjected to first processing and b) first and second processing are asynchronously executed as claimed in claims 25 and 26."*

However Charles was not relied upon for having taught the argued limitations above in claims 1 and 11. Charles was **not** cited for teaching *a) each processor executing a processing function different from one another, b) a plurality of processors executing a series of different types of processing functions, c) one processing is executed at a time on each pixel by one of the processors or d)*

processing functions are asynchronously executed as claimed in claims 1 and 11. Charles was also not cited for teaching *a) second processing on data to be processed that was subjected to first processing and b) first and second processing are asynchronously executed as claimed in claims 25 and 26.* Charles was merely cited for teaching a shared memory device for a processor/coprocessor (Charles, Column 27, lines 53-63). Therefore this argument is moot.

6) On page 10, line 28-page 11, line 13 of the Appeal Brief, Appellant argues in essence:

> *"Applicants respectfully submit that the prior art does not show, teach or suggest a) a second (image) processor for executing second processing on the data to be processed that was subjected to the first processing ... as claimed in claims 25 and 26. Orimo et al. discloses in Figure 6 an AP input/output data area (col. 5, lines 13-14), which stores data to be transmitted to other application programs in the data field 30714 (col. 6, lines 44-47). Nothing in Orimo et al. shows, teaches or suggests that this data was subjected to other processing as claimed in claims 25 and 26 (i.e. Orimo et al. discloses data passed between application programs but does not show, teach or suggest executing second processing on the data to be processed that was subjected to the first processing as claimed in claimed 25 and 26.). Rather, Orimo et al. merely discloses that data output by the application is stored in a data field and subsequently output as part of a message. In other words, the data that is output in the message of Orimo et al is result data and is not data that was subjected to first processing by a first processor."*

However, examiner notes that the cited sections of Orimo in the argument above *(col. 5, lines 13-14 and col. 6, lines 44-47)* are **not** relied upon anywhere in the rejection of the claims on appeal. Furthermore, Orimo has taught *a second processor for executing second processing on the data to be processed that was subjected to the first processing.* (Orimo, figure 1, column 2, lines 1-25, second

processor, column 11, lines 18-21) The cited portions of column 2 and column 11 could not be more clear that first processors execute first processings and output execution result data in messages to the second processor. The second processor selects a message and executes a second processing program in the second processor using the executed result data contained in the selected message. Therefore, Orimo has in fact taught *a second processor (*column 2, lines 1-25, lines 18-21, second processor*) for executing second processing on the data to be processed (column 2, lines 14-16, The second processor executes a second program.) that was subjected to the first processing (column 2, lines 6-7 and 9-16,* The second processor selects a message and executes a second processing program in the second processor using the executed result data contained in the selected message*).* Therefore this argument is moot.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tonia L. Meonske

Tonia L. Meonske 10/26/2006

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